RANDOM ACCESS MEMORY HAVING DRIVER FOR REDUCED LEAKAGE CURRENT

Abstract

One embodiment of the present invention provides a random access memory (RAM) including an array of memory cells arrange in a plurality of rows and columns, wherein access of each row is based on a wordline signal, and a wordline circuit. The wordline circuit includes a voltage node receiving a positive voltage from an external power source, a decoding node receiving a decoding signal having a state representative of an idle mode, and a driver circuit providing to at least one of the rows of memory cells a wordline signal based on the decoding signal and forming a current leakage path from the voltage node to a reference node when the decoding signal state indicates the idle mode.